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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/805,670 | 03/19/2004 | Franz Hofmann | V0195.0012 | 8567 |

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| EXAMINER | |
|---|---|
| NHU, DAVID | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2818 | |

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/805,670 | HOFMANN ET AL. | |
| | Examiner | Art Unit | |
| | David Nhu | 2818 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *1-19 and 38* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. PCT/DE02/02742.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTIONS

### *Election/Restrictions*

1. Applicant's election of Group I (Claims 20-37) **with traverse** is acknowledge. Claims 20-37 are remained for examination. Accordingly, claims 38 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Because Applicant did not distinctly and specifically point out the supposed error in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Applicants have the right to file a divisional, continuation or continuation-in-part application covering the subject matter of the non-elected claims. The traversal is on the ground(s) that see the election paper. This is not found persuasive because the fields of search for method' and device claims are NOT coextensive and the determinations of patentability of method and device claims are different, that is process limitations and device limitations are given weight differently in determining the patentablitity of the claimed inventions. Also, the strategies for doing text searching of the device claims and method claims are different. Thus, separate searches are required.

The requirement is still deemed proper and is therefore made **FINAL**.

### Drawings

2. There is no the semiconductor memory element arrangement 100 in figures 1e and 2e.

## *Claims Objection*

3. Claim 20, "**can**" should not use in the claim.

"the tunnel barrier arrangement" should be –the multiple tunnel barrier arrangement—

Claim 35, "the electrical potential; the electrical charge transmission" lack a clear antecedent basis.

## *Claim Rejections - 35 USC § 102*

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 20-37 are rejected under 35 U.S.C. 102 (b) as being anticipated by Noble et al (5,973,356).

***Regarding claim 20**, Noble, (see figures 3-13, 16-21, col. 9, lines 14-67, col. 10-13, col. 1-67), teaches a method for fabricating a semiconductor memory element arrangement, comprising: forming a first electrically insulating layer 705, 1100 on a substrate 305; forming a layer system 500, 505, 515, 520 (see figure 9), including a floating gate 805, and a multiple tunnel barrier arrangement 515, 520, 800, 900, 905 formed on the floating gate, on the first electrically insulating layer 705; forming a first trench structure 600 in the layer system, the first trench structure having first trenches 600 arranged parallel to one another and extending as far the first electrically insulating layer (see figure 9); forming a second trench structure 1300 in the layer system, the second trench structure having second trenches arranged parallel to one*

*another and extending as far the first electrically insulating layer 1605 (see figure 16), the second trenches being arranged perpendicular to the first trenches (see figures 13, 20); forming in the first and second trenches, a first gate electrode adjacent to the floating gate through which first gate electrode electrical charge is fed or is dissipated from (see figures 12, 13); forming, in the first and second trench structures, a second gate electrode adjacent to the multiple tunnel barrier arrangement, wherein through the second gate electrode an electrical charge transmission of the multiple tunnel barrier arrangement is controlled (see figures 19, 20).*

*Regarding claim 21, Noble, (see figures 11, 19), teaches forming a second electrically insulating layer on the multiple tunnel barrier arrangement; patterning the second electrically insulating layer in accordance with the first and second trench structures.*

*Regarding claim 22, Noble, (see figures 12, 19) teaches performing a first photolithography step by using a first photomask having a pattern of parallel strip-type openings which are arranged perpendicular to the strip-type openings whose width corresponding to a minimum feature size of the first trench; performing a second photolithography step using a second photmask having a pattern of parallel strip-type openings which are arranged perpendicular to the strip-type openings of the first photomask and whose width corresponding to the minimum feature size of the second trench structure.*

*Regarding claims 23-32, Noble, (see figures 1-21), teaches forming spacer 905 on the second electrically insulating layer in the first trenches; the first trenches have a smaller than the second trenches; the first and second gate electrode 325, 335 are formed from polysilicon; the*

*multiple tunnel barrier arrangement comprises a layer stack of insulating layers; the insulating layers are formed from silicon oxide or silicon nitride.*

*Regarding claims 33, 34, Noble, (see figures 9-11), teaches the semiconductor and insulating layers are formed with thicknesses.*

***Regarding claim 35**, Noble, (see figures 1-4, 3-13, 16-21,col. 4, lines 35-67, col. 5-8, lines 1-67, col. 9, lines 14-67, col. 10-13, col. 1-67), teaches a method for operating a semiconductor memory element arrangement having a first electrically insulating layer 705, 1100 formed on a substrate 305 and a layer system 500, 505, 515, 520 (see figure 9) comprising a floating gate 805 and a tunnel barrier arrangement formed on the floating gate, the layer system being formed on the first electrically insulating layer 705 and forming a multiple tunnel barrier, wherein first and second gate electrodes are formed in a first trench structure 600 formed in the layer system, the first trench structure including first trenches arranged parallel to one another and extending as far as the first insulating layer, and a second trench structure 1300 formed in the layer system, the second trench structure including second trenches arranged parallel to one another and perpendicular to the first trenches and extending as far as the first insulating layer, the method comprising: reading an electrical potential on the floating gate via the first gate electrode; and controlling n electrical charge transmission of the tunnel barrier arrangement via the second gate electrode (see figures 1-4).*

*Regarding claims 36-37, Noble, (see figures 1-4), teaches reading data of the semiconductor memory element arrangement by applying an electrical voltage to the first gate electrode with the second gate electrode; writing or erasing data of the semiconductor memory element*

*arrangement by applying an electrical voltage to the second gate electrode with the first gate electrode.*

**Conclusion**

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Gonzales'017 is cited as of interest.

7. A shortened statutory period for response to this action is set to expired 3 (three) months from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see 710.02 (b)).

8. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu, (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:00 AM to 5:30 PM.

*The fax phone number for the organization where this application or proceeding is assigned is (571)273-8300.*

*Information regarding the status of an application may be obtained from the patent application information retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).*

David Nhu

September 23, 2006